Atomic-scale device fabrication strategy

Within the Atomic Fabrication and Crystal Growth Program we have developed a novel strategy for the realisation of atomic-scale devices in silicon using a unique combination of STM based lithography, phosphorus doping, MBE crystal growth, and conventional optical lithography. One of the key milestones has been the development of a registration technique [1] that allows the alignment of macroscopic electrodes to the atomic scale devices elements and solves the engineering problem of making electrical contact to a STM-patterned device (Figure 1).

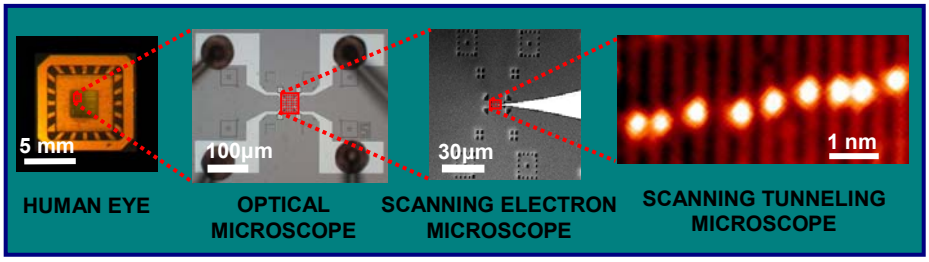

Figure 1: Range of technologies and length scales that have been aligned compatibly from optical to scanning electron to scanning tunnelling microscopes. Our unique registration technique bridges the gap between the atomic and micron length scale.

The overall fabrication strategy for the realisation of atomic-scale devices is outlined in Figure 2.

Initially, registration markers are etched into the silicon substrate and subsequently used to align the STM-patterned buried dopant layer (Figure 2a) [1]. Optimisation of STM-based hydrogen lithography down to the atomic scale has enabled us to adsorb single PH_3 molecules at selective sites on the silicon surface (Figure 2b) [2].

A critical anneal incorporates individual phosphorus atoms into the silicon surface (Figure 2c) before thermal removal of the hydrogen resist (Figure 2d) [3,4].

Separately we have shown that a sheet of phosphorus atoms can be encapsulated using silicon MBE at low temperatures [5] minimizing dopant diffusion and segregation out of the patterned regions (Figure 2e).

Finally the sample is removed from the ultra-high vacuum and the registration markers are used to align surface electrodes to the buried dopant layer (Figure 2f).

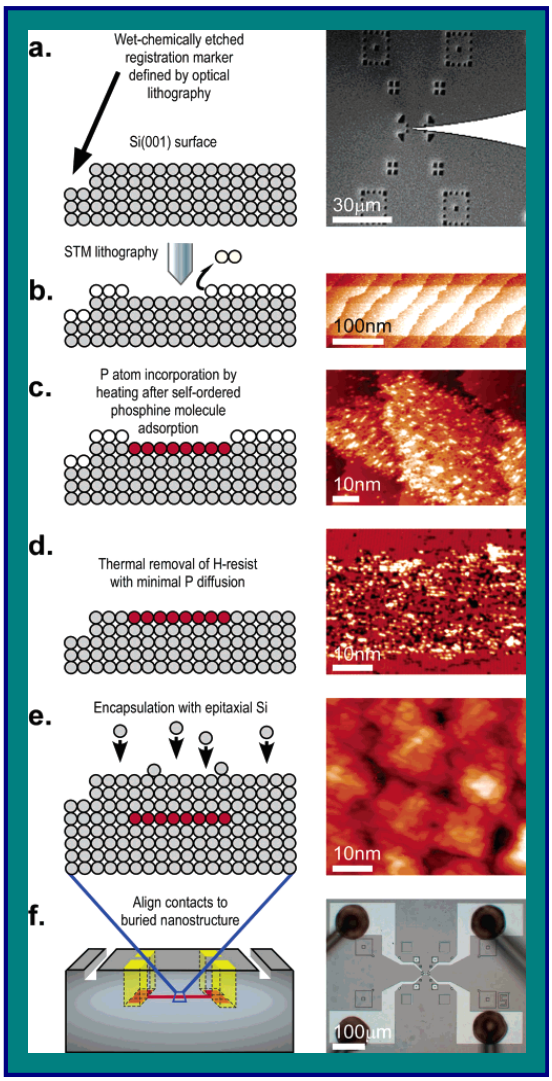

Figure 2:Device fabrication strategy for the creation of Si:P atomic devices using scanning probe microscopy.

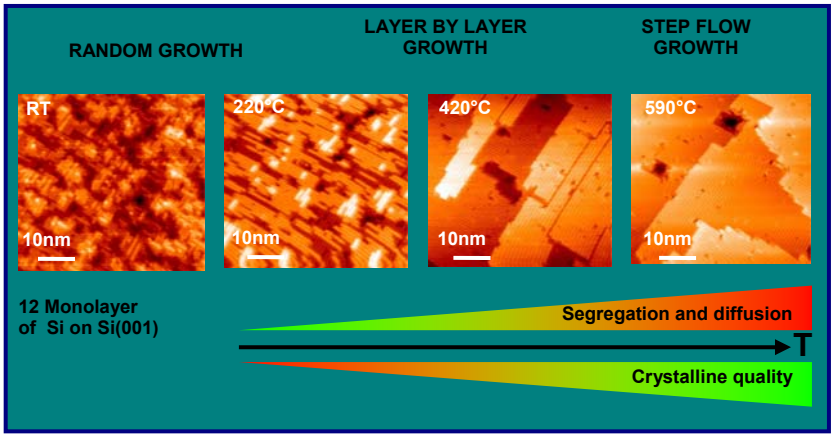

Figure 3: A detailed STM study of the structural properties of Si homoepitaxial growth shows that epitaxial growth can still be achieved at room temperature. δ-doped layers encapsulated at different growth temperatures have shown that minimal dopant segregation and complete electrical activation can be achieved after encapsulation at RT and 250°C. Silicon encapsulation of P atoms at 250°C results in a mobility of ~61cm^2/Vs and a phase coherence length of 72nm at 4.2K.

Currently we are developing a low temperature silicon dioxide growth process so that we can align surface gates to buried STM-patterned dopants for the control of the atomic-scale devices. We have recently demonstrated transistor action of a MOSFET fabricated using this new oxide growth technique, an important step towards gating of STM-patterned atomically precise P dopant devices in Si.

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[4] N.J. Curson *et al.* Phys. Rev. B **69**, 195303 (2004)

[5] L. Oberbeck *et al.* Appl. Phys. Lett. **81**, 3197 (2004)