2D electron transport

One of the advantages of the STM approach to P in Si device fabrication is that it is possible to investigate the local electronic environment of the 2D plane of dopants using STM and directly relate this to the electronic transport mechanisms determined from magneto-transport measurements. Initial studies concentrated on developing a low temperature encapsulation process to prevent segregation of the P atoms in the δ-doped layer. Four terminal magneto-transport measurements demonstrated complete electrical activation of the dopants [1] with minimal segregation [2]. Since then we have investigated the electronic properties of two-dimensional P in Si δ-doped devices for a variety of dopant concentrations, see Figure 1. These results demonstrate that ballistic transport can only be observed in devices limited to a length scale of several nm whilst those exploiting phase coherence transport can be at least an order of magnitude larger [3].

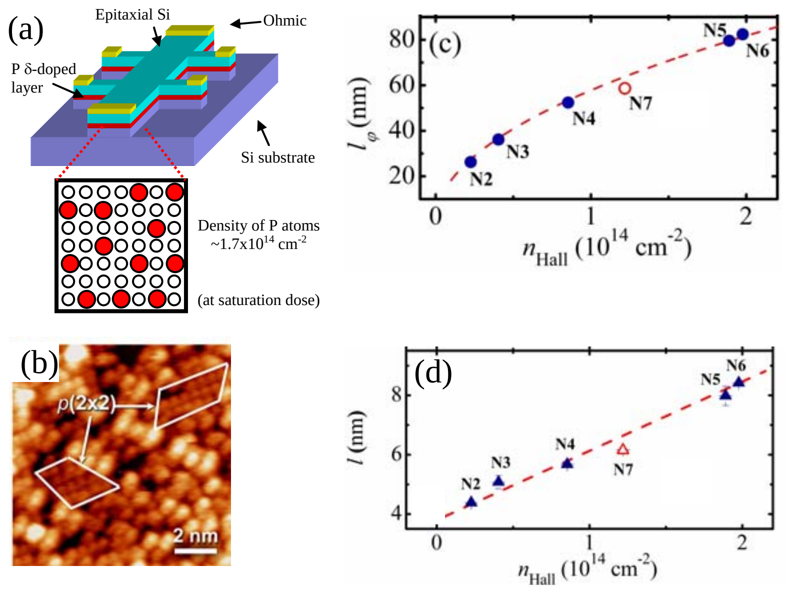

Figure 1 (a) a schematic of a P:Si δ-doped Hall bar sample, (b) a STM image of a saturation dosed sample showing regions of local p(2 x 2) PH_2 ordering; (c) phase coherence length and (d) mean free path as a function of carrier density from 2.7 x 10^{13} cm^{-2} to 2 x 10^{14} cm^{-2}.

Recently we have used the STM to pattern the dopants within the 2D plane as shown in Figure 2 (a). Here we show a 200 nm x 100 nm channel between two highly P-doped source-drain leads into which we pattern an ordered array of highly P-doped dots approximately 6 nm in diameter with a 10 nm period by STM lithography. After phosphine adsorption each dot contains ~50 P atoms. We then encapsulate the array with ~25nm epitaxial silicon grown at low temperature by MBE.

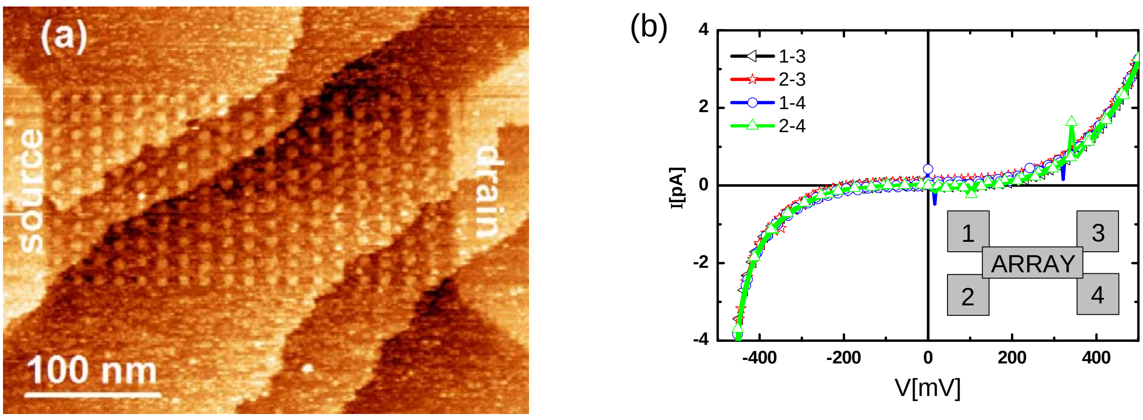

Figure 2: A filled state STM image of (a) a H:Si (100) surface patterned by STM into an ordered dopant array between source and drain leads for electrical measurement. (b) 2-terminal I-V characteristics of the ordered array device at 4 K show that a minimum voltage threshold of ± 250 mV must be reached before conduction occurs across the array.

Measurements of the current-voltage characteristics across this device shown in the right hand side of this figure confirms non-linear behaviour requiring a source-drain voltage of ±250mV to be applied before conduction can occur [4]. These I-V characteristics across all contacts, are highly symmetric indicating that the electrical characteristics of the array are independent of the contact resistances at 4K. The results are consistent with a barrier to electron transport due to the separation of the dopants within the 2D plane confirming that the STM-patterning has survived the encapsulation process. Current work is focussing on reducing the number of dopants down to the single atom level.

[1] K.E.J. Goh *et al.,* "Effect of encapsulation temperature on Si:P δ-doped layers", Applied Physics Letters **85**, 4953-4955 (2004)

[2] L. Oberbeck *et al.,* "Measurement of phosphorus segregation in silicon at the atomic-scale using STM", Applied Physics Letters **85**, 1359 (2004)

[3] K.E.J. Goh *et al.,* "Influence of doping density on electronic transport in degenerate Si:P δ-doped layers", Physics Review B **73**, 035401 (2006)

[4] W. Pok *et al.,* "Electrical Characterization of Ordered Si:P Dopant Arrays", IEEE Transactions on Nanotechnology **6**, 213 (2007)