# Materials Program

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**PROGRAM DESCRIPTION**

The aim of this program is to investigate the types and quantities of defects produced during the fabrication of silicon-based quantum computer related devices by the top-down approach. This program advises the Centre on defect minimization strategies and ensures the materials are kept to the highest quality.

## 1. 2009 Overview

The Materials Program utilizes and continues to develop a number of defect characterization techniques in order to inform the Centre on optimal processing strategies. $Si$-$SiO_2$ interface trap densities continue to be produced at an acceptably low level. The fixed oxide charge and the Al-Si work-function difference of gate oxides have been measured this year. The processing strategy used to fabricate an electrically detected magnetic resonance (EDMR) device completely fabricated with ion implantation techniques is also being studied through a number of experiments.

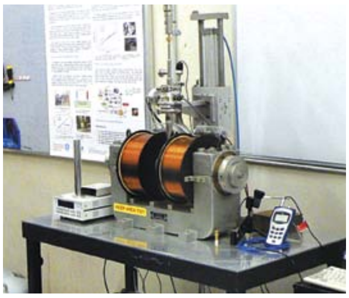

**FIGURE 1**

The Hall effect system in the electrical characterization laboratory. It consists of a Newport Instruments 1 tesla electromagnet, Keithley electronics and a Janis He/N dewar and probe system.

Hall measurement capabilities have also been realized this year. The Hall system (shown in Figure 1) will be routinely used to monitor the dopant activation and mobility of ion implanted materials. Both van der Pauw and Hall bar geometries are possible at measurement temperatures ranging from 20 - 320 K. The Hall system is also equipped with a 1 Tesla electro-magnet. Various device structures are currently being developed. A specialized Hall bar metal oxide semiconductor field effect transistor (MOSFET) with a top gate that may also be used as a micro-wave antenna for EDMR is currently being investigated. An aperture in the gate will allow optical-EDMR measurements.

## 2. Characterization of MOS capacitors and defects

Long-term trends in oxide quality can now be monitored with the compilation of 6 years of CV/DLTS data. Standard high-quality oxides with a nominal thickness of 5 nm average 5.7 nm with a 0.8 nm standard deviation. Since the furnace plumbing was improved in 2006, the interface trap density slowly came down over 2007 and since then has consistently been in the low $10^{10}$ /cm$^2$ range. Such analysis will aid us in monitoring the reproducibility of the high-quality oxides and identifying any problems in oxide growth or processing at an early stage.

Collaboration with Sandia has led to an increased understanding of Centre oxides. The High/Low frequency capacitance-voltage (CV) technique favoured by Sandia and the DLTS technique employed by us showed excellent agreement. Slight differences could be attributed to the capture cross-section value of interface states needed for the DLTS analysis. An artefact in weak inversion of the CV profiles of our test structures also limited the accuracy of the Sandia analysis. The source of this artefact has since been identified as being a parallel capacitance caused by the field oxide and has been eliminated from subsequent test structures. This has resulted in greater confidence and accuracy of the CV/DLTS measurements.

The quality of Centre materials has also been characterized via the PiN devices that the Ion Beam Program utilizes for deterministic single $P^+$ implantation detection. These devices are integrated into structures that also contain MOSFET devices used to probe the Si:P system. The relationship between defects and detection capabilities was explored. It was found that in some devices, processing-induced electrically active defects were present and contributed significantly to the noise of the device during implantation. Current-voltage measurements showed a characteristic generation current in reverse bias while DLTS showed the presence of several kinds of traps that caused the unwanted leakage current. These studies will continue in 2010 in the hope of improving the detector capabilities and design. The effect of these bulk defects, if any, on the coherence of spin and charge based systems in the MOSFET will be further explored.

## 3. Fixed Oxide Charge

The field oxides grown by the Centre by a wet oxidation process were found to contain a high enough concentration of fixed oxide charge to induce a 2D electron gas (2DEG) under the $Si$-$SiO_2$ interface. $P^+$ guard rings were incorporated into the latest device designs to inhibit any possible inter-device leakage current through this 2DEG. In 2009, the first measurement of fixed oxide charge in the gate oxide was performed. Although these defects are not in electrical communication with the underlying substrate, they can cause a threshold voltage shift in MOSFET devices. It is critical to keep this effect to a minimum in order to ensure the consistent operation of Centre MOSFET devices.

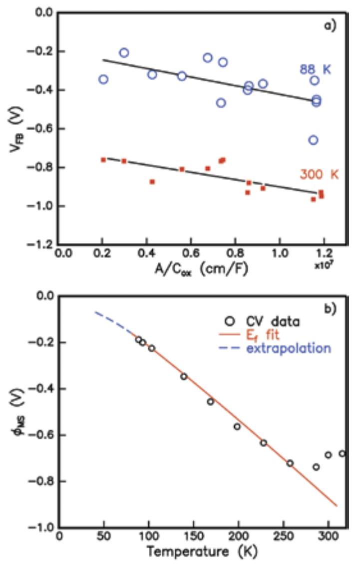


**FIGURE 2**

(a) The flatband shift as a function of of $A/C_{ox}$ determined from the Capacitance-Voltage profiles of a single gate oxide having undergone various etches to thicknessess. (b) The Al-Si workfunction difference as a function of temperature. The fit is based on the shift in the Fermi level in Si. This has been extrapolated down to 40 K beyond which little variation is expected due to Fermi level pinning to the dopant band.

Figure 2a shows the flatband voltage shift (the gate bias required to achieve flat bands) as a function of the oxide thickness at 80 and 300 K. From the gradient of these curves the fixed oxide charge was found to be 1.3 x $10^{11}$ /cm$^2$ in the gate oxides grown at 1000°C. The fixed oxide charge may not be evenly distributed through the oxide but increase as the $Si/SiO_2$ interface is approached. This is due to the strain and lattice mismatch that exists at the interface. It is therefore not surprising that the fixed oxide charge is not much less than the field oxide ($1.9 \times 10^{11}$ /cm$^2$). There is evidence that this value can be improved with implantation plus a rapid thermal anneal.

The fixed oxide charge density does not vary with temperature. However, the offset of Figure 2a seems to have a large temperature dependence which is due to a temperature dependent variation in the Al-Si work-function difference. Figure 2b shows this variation with temperature. The Fermi level shift in the Si with temperature could model this behaviour well but a scaling factor had to be incorporated. The value was then extrapolated down to 40 K using this model where most standard semiconductor parameters are valid. Below this temperature it is expected that the Fermi level will be pinned to the dopant band and hence the Al-Si work-function difference will not change will temperature. This variable is important for the accurate simulation of Centre MOSFET behaviour with gate bias at low temperatures. The value has been incorporated into various simulations undertaken by the Centre.

## 4. Formation of EDMR Devices Via Implantation

The EDMR device proposed in 2007 by the Quantum Measurement program is an important Centre device that can be used as a spectroscopic tool to probe the Si:P system directly. In 2008 the Centre also suggested that this device be coupled with a single electron transistor (SET) to form a qubit with charge-based spin read-out. To fully utilize its potential the device must be fabricated using ion implantation technology. To this end, we have designed a number of ongoing experiments to realize this fully implanted EDMR device.

In the first instance, As was implanted through a 20 nm oxide into both test MOS capacitors and the channels of EDMR devices to determine the optimal processing parameters for dopant activation in a MOSFET channel. The source and drain were formed by P in-diffusion. The As is expected to have four hyperfine peaks whereas P has two given the difference in its nuclear spin. Therefore, it can be observed whether P in the tails of the P doped leads contributes to the EDMR signal.

Various post-implantation anneal strategies were considered including a rapid thermal anneal (RTA) at 1000°C for 5 s in a nitrogen ambient, a 950°C, 30min furnace anneal (FA) in a forming gas ambient (95% $N_2$, 5% $H_2$) and a combination of the two (RTA+FA). Figure 3 shows the CV obtained from the MOS capacitors having undergone the three different annealing strategies. The slight shifts in voltage are attributed to fixed oxide charge. Although the FA is most efficient at activating the dopants indicated by the increase in the inversion capacitance, a comparatively large amount of fixed oxide charge remains after the anneal. The fixed oxide charge is estimated to increase by $2.9 \times 10^{11}$ /cm$^2$ whereas the RTA sample results in an increase of $1.6 \times 10^{11}$ /cm$^2$.

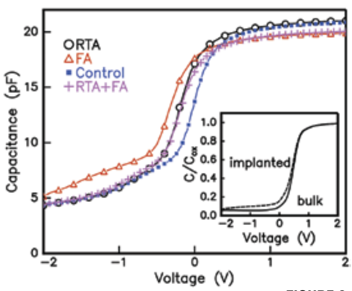


**FIGURE 3**

Capacitance–voltage curves of processed MOS test capacitors measured with an AC frequency of 1 MHz. The measurement temperature was 300 K. The inset shows the simulated CV of a bulk doped (solid line) and As implanted wafer (dashed line).

Evidence of minority carriers was also found in the inversion capacitance temperature scan as shown in Figure 4. A peak is observed at a temperature where an inversion layer is formed. At temperatures above this peak the capacitance transient is dominated by minority carrier generation–recombination. For our usual good quality oxides this peak appears near room temperature. Preliminary results suggest that thinning of the low-quality field oxide during processing is the cause. A field produced by the gate shifts the Fermi level to a position where hole generation is more likely. The role of minority carrier traps at the low temperatures (<4 K) where FET measurements are made is not yet known.

The RTA after implantation resulted in the lowest fixed oxide charge and interface trap densities while also limiting the As diffusion. The EDMR device showed characteristic turn-on behaviour and minimal leakage current. This suggests that implantation through an oxide layer followed by an RTA is a viable and realistic means of successfully fabricating spin-dependent transport FETs. However, the hyperfine lines from As dopants were not observed. It is suspected that either the As concentration was too high or strain and the presence of other dopants in the material inhibited the EDMR signal.

Presently, As and P have been implanted at a range of fluences resulting in peak concentrations of $1 \times 10^{15} - 1 \times 10^{18}$ /cm$^3$. The lower fluences will eventually be an ideal test of the sensitivity of EDMR devices. In the quantum device proposed by the Centre, a single P donor would be implanted under the radio frequency gate. A value of the exchange coupling between implanted dopant atoms may also be determined for the higher fluences. Furthermore, these experiments will provide key data for the fabrication of the EDMR devices. Preliminary DLTS results show excellent oxide quality and high dopant activation.

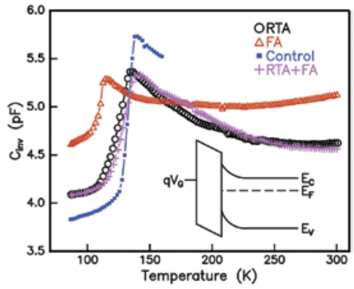


**FIGURE 4**

Inversion capacitance at a gate bias of −2 V as a function of temperature. The inset is a schematic of the band structure of the MOS capacitor during the temperature scan.

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