

Materials Program

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PROGRAM DESCRIPTION

The aim of this program is to investigate the types and quantities of defects introduced into silicon under the processing conditions used to fabricate a phosphorus in silicon quantum computer by the top-down approach and to advise the Centre on methods of defect minimisation.

1. 2008 Overview

Deep level transient spectroscopy (DLTS) continues to play a central role in monitoring the quality of the materials produced by the Centre. Interface trap densities continue to be produced at an acceptably low level. With the technique now in routine use, various aspects of the fabrication process have been studied. In addition, the first measurement of the fixed oxide charge was performed. This measurement has in part prompted a more robust MOS design containing guard rings to shield against any leakage between adjacent devices.

Process optimization using these techniques has also been applied to aspects of the spin-dependent transport device produced by the Quantum Measurement program last year. In a variation on the device, the appropriate fabrication steps were determined for the formation of arsenic leads by implantation through an oxide. Through collaboration with this program it is hoped the device can be further developed as a promising means for qubit control.

Brett Johnson started as a post-doctoral research fellow with the Centre this year. He brings a background in ion implantation induced defect characterisation to the Centre and is currently working to identify defect minimization and measurement strategies in quantum device fabrication.

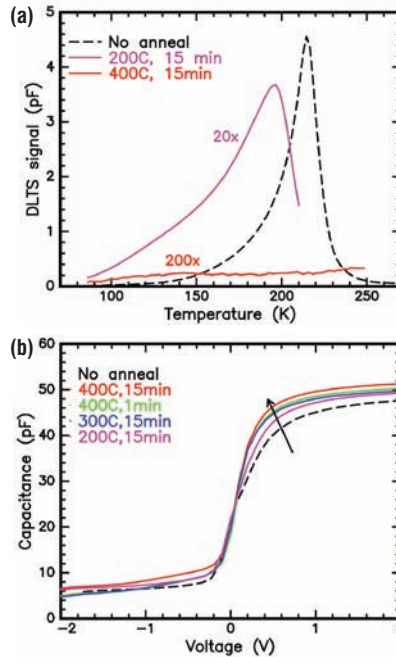


FIGURE 1
 (a) The raw DLTS signal as a function of measurement temperature showing a large defect peak (dashed line) which disappears after a 400°C, 15 minute anneal. (b) High-frequency capacitance-voltage (CV) profiles for a MOS capacitor with an oxide thickness of 6.4 nm. The C-V profile approaches the ideal low defect curve (most abrupt profile) as the post metallization anneal temperature is increased.

2. Post-Metallization Anneal

In 2008, the importance of the post-metallization anneal in our device fabrication protocol has been investigated. Figure 1(a) shows DLTS data from a metal-oxide-semiconductor (MOS) structure after aluminium gates were evaporated onto the oxide surface but prior to any post-metallization annealing. A large asymmetric peak was found which indicates a large concentration of defects rendering a full DLTS analysis unfeasible. The peak shows some unusual characteristics and is not indicative of a standard bulk or silicon-oxide interface type defect. This has hindered its identification. The peak shown in Figure 1(a) disappears after an anneal at 300°C for 15 minutes. However, the interface defect densities are still quite high (not shown). An anneal at 400°C for 15 minutes is required to remove the peak and reduce the interface trap density to an acceptable level. These measurements have confirmed the importance of this anneal in our device processing strategy.

Figure 1(b) shows the corresponding capacitance-voltage (CV) profiles. The large peak in the DLTS data manifests in the CV as a stretching of the profile and a decrease in the capacitance at positive voltages. With subsequent annealing it can be seen that the CV profile approaches the ideal MOS CV profile (as indicated by the arrow in Figure 1(b) with the low trap density usually associated with recent Centre oxides. Standard and accurate analysis can be

performed with such an oxide. This work illustrated the importance of the final post-metallization anneal and shows that CV measurements can be used as a quick indicator of oxide quality before a full DLTS measurement is undertaken.

3. Fixed Oxide Charge

The increasing importance of silicon quantum dot structures in our device program has required some attention to be paid to the presence of fixed oxide charge in our devices. Fixed oxide charge arises from structural defects in the oxide and depends on the oxide growth parameters. Although these defects are not in electrical communication with the underlying substrate, the fixed oxide charge can induce the formation of a 2D electron gas under the Si-SiO₂ interface that can interfere with device operation. Preliminary CV measurements have been performed on MOS capacitors in order to determine the fixed oxide charge in thick field oxides grown by the Centre. The effect of a post-oxidation forming gas anneal on the fixed oxide charge has also been determined.

Figure 2(a) shows the CV measurements from the annealed sample with various oxide thicknesses produced by etching the as-grown wafer for various times. The flat band voltage of these curves as a function of the oxide thickness can be used to measure the fixed oxide charge density as shown in Figure 2(b). This method yielded fixed oxide charge densities of 2.1×10^{11} cm⁻² and 1.9×10^{11} cm⁻² for the un-annealed and annealed samples respectively. These densities are reasonably low but may not be low enough for our quantum devices so guard rings have been incorporated into new more robust device designs to inhibit any possible inter-device leakage current.

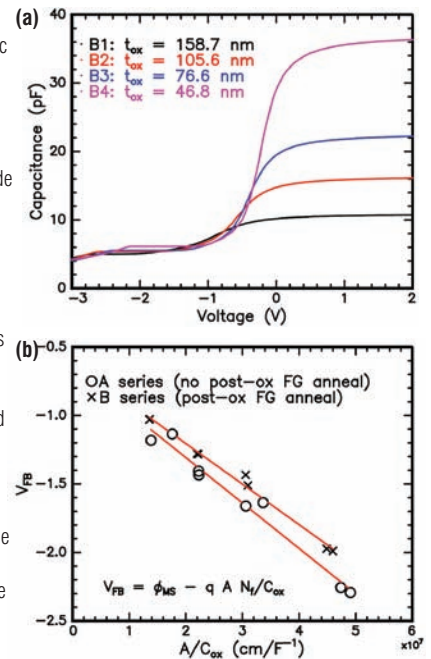


FIGURE 2
 (a) Capacitance-Voltage profiles for the field oxide having undergone a post-oxidation anneal and various etches to thicknesses indicated on the figure. (b) Flat band voltage determined from the C-V curves as a function of the A/Cox for the etched field oxides.

4. Measurement of Integrated Test Structures

In 2008, integrated test structures were incorporated into device wafers allowing defect characterization measurements to be performed on actual device oxides. From measurements on such devices it will be possible to determine whether any of the quantum device fabrication steps affect the quality of the oxide. These structures are fabricated on Topsil wafers which have a resistivity of $10,000 \Omega \cdot \text{cm}$. With such a high resistivity, standard DLTS was not possible. Alternative techniques have been explored to measure these structures.

Figure 3 shows the CV profiles measured with probe frequencies of 1 MHz using our standard system from SULA and 1 kHz using an Andeen-Hagerling capacitance bridge. A large decrease in the capacitance is found in the accumulation region (positive voltages) for the 1 MHz CV measurement. Details about the oxide cannot be extracted from CV curves using the standard method. The discrepancy between these two measurements is due to the high resistivity of the substrate.

A greater understanding of the measurement of these structures can be achieved with capacitance simulations using Technology Computer Aided Design (TCAD) from ISE. Using a simple 2D mesh based on the integrated test structures it was possible to reproduce the observed CV profiles.

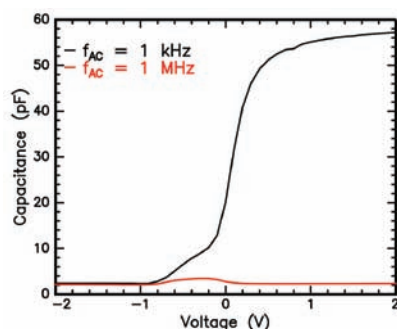


FIGURE 3

Capacitance as a function of gate bias performed with the usual 1 MHz probe frequency and 1 kHz probe frequency from an Andeen-Hagerling capacitance bridge. An oxide thickness was calculated as 4.9 nm from the 1 kHz data. The effect of series resistance can be seen in the 1 MHz case.

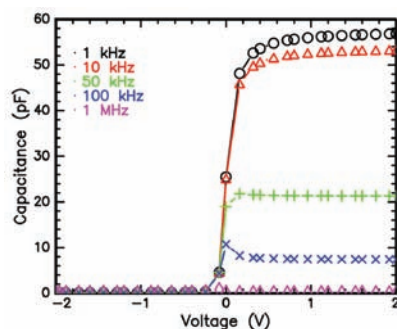


FIGURE 4

Simulated CV curves for the integrated test structure for various AC probe frequencies. As the frequency increases series resistance begins to reduce the capacitance in accumulation. For frequencies of 1 kHz and below the maximum capacitance does not vary.

Figure 4 shows simulated CV profiles for the integrated test structure for various AC probe frequencies. As the frequency increases series resistance begins to reduce the capacitance in accumulation. The series resistance of this device does not affect the maximum capacitance obtained with a 1 kHz probe frequency. Therefore, the oxide thickness can still be reliably determined. Such simulations may be useful for the design of future structures for measurement.

In addition to measuring the capacitance of the MOS capacitor the Andeen-Hagerling capacitance bridge also measures the conductance. The possibility of determining the interface trap densities with conductance measurements has been explored. Figure 5 shows the conductance-voltage (GV) profiles for various measurement temperatures. There are contributions to this profile from many different effects including series resistance and generation-recombination through bulk and interface traps. The height of the interface trap peak, which is close to zero volts in the figure, can be related to the concentration of interface traps. An interface trap density of $4 \times 10^{10} \text{ eV}^{-1} \cdot \text{cm}^{-2}$ was determined which is consistent with expectation. An independent experiment with current transient spectroscopy is currently being developed.

5. Focussed-ion beam cross-sectioning of device structures

FIB cross-sectioning of quantum device structures continues to be an extremely important diagnostic tool for the Centre. This series of images shows details of a double-island gate defined silicon quantum dot structure that is currently being studied in the quantum measurement program. Figure 6 is an expanded view of the device while Figure 7 shows a close-up of one of the double quantum dot structures revealing details of the finger structures used to define the double quantum dots and the overlying top gate. Figure 8 is a bright-field transmission electron micrograph of a cross-section through the three aluminium gate fingers showing details of the aluminium oxide interfacial regions surrounding each finger. These provide electrical isolation between the various levels of metallisation and they are thicker and less uniform than expected. The relevant processing steps are being examined to see if the outcome

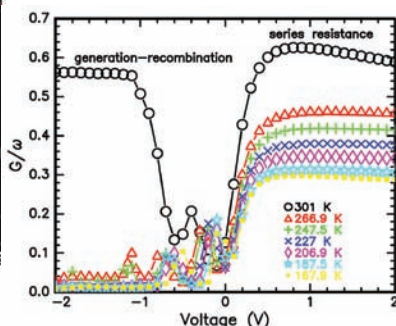


FIGURE 5

Conductance as a function of gate voltage. Contributions from series resistance and generation-recombination through bulk and interface traps are observed.

can be improved for later generations of devices. In addition, knowledge of the actual oxide thickness and uniformity are being fed into the device measurement program.

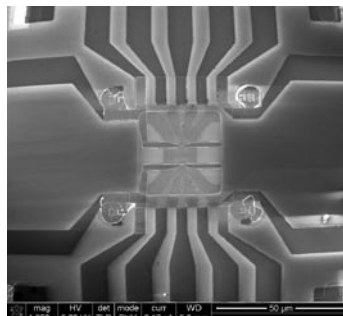


FIGURE 6

Scanning electron micrograph of double quantum dot gate defined silicon quantum dot structure.

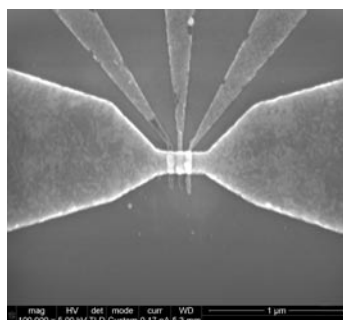


FIGURE 7

A close-up of one of the double quantum dot structures revealing details of the finger structures used to define the double quantum dots and the overlying top gate.

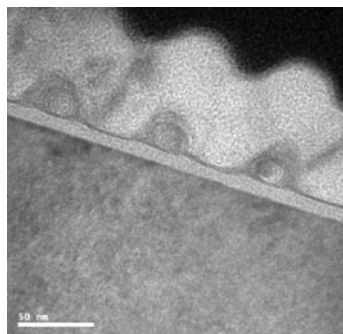


FIGURE 8

Transmission electron microscopy image of a cross-section through the three aluminium gate fingers showing details of the aluminium oxide interfacial regions surrounding each finger which provide electrical isolation between the various levels of metallisation.

Bibliography

- Johnson B.C. & McCallum J.C. 2007. Dopant-enhanced solid-phase epitaxy in buried amorphous silicon layers. *Physical Review B*. **76**: 0452161-04521612.
- Villis B.J. & McCallum J.C. 2007. Angular dependence of defect formation in H-implanted silicon studied using deep level transient spectroscopy. *Nuclear Instruments & Methods in Physics Research Section B - Beam Interact with Materials and Atoms*. **257**: 212–216.
- Johnson B.C., Gortmaker P & McCallum J.C. 2008. Intrinsic and dopant-enhanced solid-phase epitaxy in amorphous germanium. *Physical Review B*. **77**: 2141091-21410912.
- Johnson B. C., Caradonna P & McCallum J. C. 2009. Dopant enhanced H diffusion in amorphous silicon and its effect on the kinetics of solid phase epitaxy. *Materials Science and Engineering B*. doi:10.1016/j.mseb.2008.11.047.