

## Ion Beam Program

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### PROGRAM DESCRIPTION

The ion beam program provides a high precision ion implantation process for the top-down quantum computer device fabrication strategy. In 2008 the ion beam program team collaborated closely with the team of the Quantum Computer Device Program in the construction of a large number of devices. These produced a large amount of data from the quantum measurement program which is presently being analysed. Through the years 2007 and 2008 we made steady progress in the implementation and integration of a nanometre scale step-and-repeat system in the Colutron single ion implantation facility to create precision arrays of single atoms. This system will be used for the construction of multiple qubits and also for the fabrication of devices to test the coherent transport by adiabatic passage (CTAP) protocol. We also provided a crucial service through the well-established ion beam analysis techniques including ion beam induced charge (IBIC) and RBS depth-profiling analysis in our laboratory. The detailed understanding gained from the Ion Beam Analysis effectively helped to resolve some challenging engineering issues by providing crucial information for device optimisation processes. We also explored a new potential application for the single ion implantation technology to conventional CMOS devices.

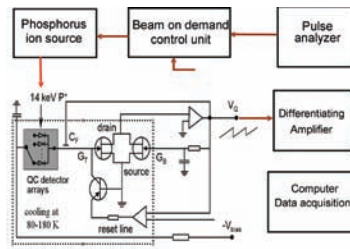


FIGURE 1

A schematic layout of the single ion implantation system.

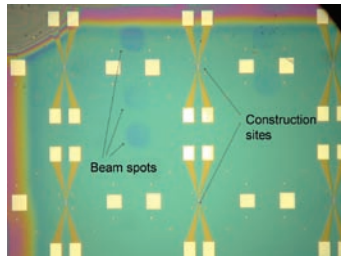


FIGURE 2

Optical image of the device LAD2-Q1 which was processed with timed implantation. The PMMA mask reveals beam spots caused by 14 keV P<sup>+</sup> ion irradiation used for alignment. The beam spots have a diameter of nominally 250 μm.

### 1. Routine ion implantation operation

The ion beam program team maintained successful ion implantation operation and provided high quality ion implantation processes for the top-down fabrication of qubit devices leading to quantum measurement. Figure 1 shows the well-established single ion implantation operation system, which integrates on-chip detector arrays with associated signal processing circuitry for the single ion implantation into high purity silicon.

Devices containing just a few donors per device could also be fabricated by controlling the implantation ion dose through measuring the ion charge collected over a period of time, named "timed implantation". Figure 2 displays a silicon chip processed with the timed-implantation operation. The beam location and size was calibrated by irradiating several areas with relatively large ion fluences which results in ion beam modification of the PMMA allowing the regions to be observed optically. The current beam alignment system has an alignment accuracy of about 100 micrometers which is sufficient for us to independently target individual devices on the chip.

### 2. Implementation of step-and-repeat system for scale up single atom array construction

A key goal for the ion beam program is the implementation of the step-and-repeat concept for the fabrication of arrays of single atoms in silicon. Figure 3 shows

the evolution of concept from 2007 to 2008. Two perpendicular slotted apertures locate individual atoms during ion implantation, one piezoelectrically driven nanostencil consisting of an aperture in a Si cantilever and the opposing slot patterned into PMMA on the substrate. In 2008 the existing concept was refined by the development of methods for precision alignment of the nanostencil with the substrate. A prototype system was developed (see Figure 4) to test the operation of a scanned nanostencil masking a beam of keV ions. The recently acquired Attocube™ three axis positioning stack holds the nanostencil perpendicular to the incident ion beam. LN<sub>2</sub> cooling of the detector substrate has not been included in the first prototype. Shown in Figure 5, the apparatus has been used to perform timed exposures using a 250 μm diameter 14 keV Ar<sup>+</sup> ion beam in PMMA. The FEI Nova dual beam FIB/SEM was used to fabricate the nanostencil by ion milling and back-filling with Pt to reduce the aperture width to less than 100 nm. SEM micrographs in Figure 5 show an aperture less than 60 nm wide which is approaching our design goal of 20 nm. The next step is to integrate the nanostencil with the single ion detection system which is a major goal for 2009. However, the concept was already demonstrated in 2008 using higher energy 0.5 MeV He<sup>+</sup> ions to construct a one dimensional map of a PMMA structure on the surface of a Hamamatsu™ Si photodiode detector (Figure 6). A Nanonics™ nano-positioning stage stepped a 50 nm aperture relative to the detector substrate which collected the pulse height spectrum at each location. Ions striking the detector through a gap in the PMMA produced a full energy pulse, while ions passing through the PMMA produced a reduced energy pulse. The pulse height spectra were plotted as an intensity map as a function of cantilever position revealing the detail of the patterned PMMA surface.

### 3. Ion beam induced charge analysis and ion damage effect

A crucial aspect of our technique for inserting single atoms is the on-chip detector. We have used the ion beam induced charge (IBIC) analysis method to optimise the detector design and to evaluate the device fabrication process. Our method of single ion event detection relies on the transport of ion impact induced charge and it is essential to achieve charge collection efficiency (CCE) close to 100% in the qubit construction zone. As we

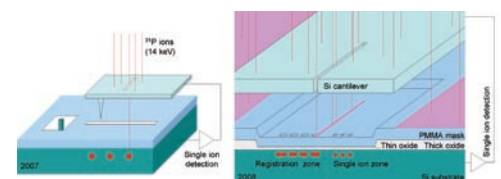


FIGURE 3

The evolution of the step-and-repeat concept for the construction of ordered arrays of single atoms in Si.

approach the goal of making devices with arrays of atoms, the stability of the CCE value with the accumulation of ion impact damage is of significant interest. To address this issue we performed IBIC analysis on standard PIN detectors to measure the CCE as a function of

ion fluence (see Figure 7). With a typical reverse bias voltage of 20 V the detector yielded initially 100% CCE with 2 MeV He<sup>+</sup> ions, but it decreased by about 5% after a fluence of  $2.0 \times 10^{15}$  ions/cm<sup>2</sup> with an associated increase in leakage current.

However we found it was possible to regain 100% CCE by simply increasing the bias voltage to compensate for the voltage drop caused by the increased leakage. Post implantation AFM imaging (Figure 7) shows no evidence of physical damage in the device. This work shows that 100% CCE can be maintained by simply increasing the detector bias voltage with increasing fluence to maintain the electrical field strength in the construction zone.

#### 4. RBS characterisation of metallisation structure in silicon interface

Detailed three dimensional characterization of device electrode structures is essential for developing the sophisticated fabrication methods for our quantum computer devices. With IBIC, Rutherford Backscattering Spectrometry (RBS) is an additional ion beam analysis technique that can provide this information. RBS analysis is insensitive to electronic properties but is a very powerful method for providing detailed knowledge of the elemental, compositional and structural details of metal films and silicon devices. Previously we applied RBS to study metal diffusion in silicon and explored a safe window of annealing temperatures. This year the RBS method was applied in the investigation of a metal-silicon Schottky structure. Thin PtEr metal layers were deposited on silicon samples and treated under different conditions. Five samples were processed under various conditions and were then depth-profiled by RBS analysis which revealed that the silicide formation was not very successful and that a new processing strategy would be required to form such silicides.

#### 5. Conclusion and Future Developments

The devices fabricated with the top-down strategy continued to provide interesting data on the manipulation of single electrons in nanoscale devices containing single or a few atoms. We have made significant progress in the implementation of the step-and-repeat system in our existing Colutron single ion implantation facility. We plan further improvements in the single ion detection system toward higher signal-to-noise ratio for lower energy ions, and there also remain challenging engineering problems that need to be fully addressed for successful operation of the step-and-repeat system. We will also expect to see more progress in the fabrication of avalanche PIN detectors for advanced single ion implantation applications, through collaborations with our colleagues in UNSW and with collaborators overseas.

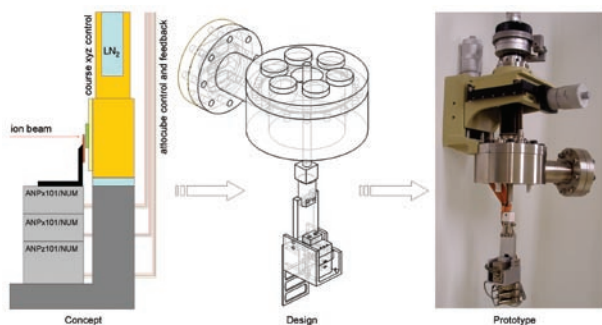


FIGURE 4

The step-and-repeat implantation stage showing the chip holder and the mounting stage designed to be integrated with the single ion implantation beam line.

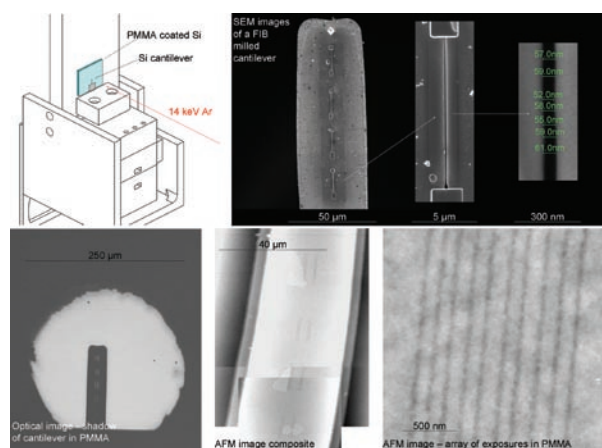


FIGURE 5

Tests of the prototype step-and-repeat system using 14 keV Ar<sup>+</sup> ions to make replicas of the nanostencil in PMMA. Clockwise from top left: Schematic of the system, SEM images of the nanostencil showing a sub-60 nm slot, replica of the nanostencil in PMMA confirming the clear passage of ions through the slot, AFM images of replicas of the nanostencil in PMMA.

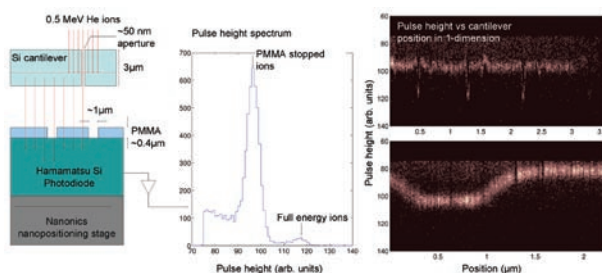


FIGURE 6

Tests of the alignment strategy for the step-and-repeat system by performing sub-50 nm IBIC on a patterned substrate.

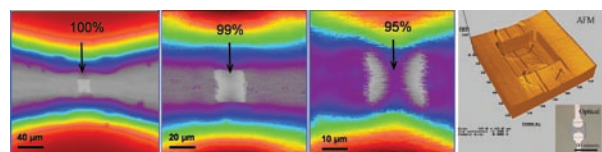


FIGURE 7

IBIC efficiency maps of the construction site showing decrease with fluence; AFM image of the central part of the PIN detector previously studied by IBIC analysis. The AFM image revealed a smooth surface condition at the detector's centre area. No surface modification by ion beam damage is visible. The lateral scan size is 65 by 65 μm. An optical image of the device is inserted at the lower and right corner of the figure; the ion entrance window area made with a 5 nm SiO<sub>2</sub> layer is clearly visible at the center of the device.