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Scanning probe microscopy for silicon device fabrication

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We present a review of a detailed fabrication strategy for the realisation of nano and atomic-scale devices in silicon using phosphorus as a dopant and a combination of ultra-high vacuum scanning probe microscopy and silicon molecular beam epitaxy (MBE). In this work we have been able to overcome some of the key fabrication challenges to the realisation of atomic-scale devices including the identification of single P dopants in silicon, the controlled incorporation of P atoms in silicon with atomic precision and the minimisation of P segregation and diffusion during Si encapsulation. Recently, we have combined these results with a novel registration technique to fabricate robust electrical devices in silicon that can be contacted and measured outside the ultra-high vacuum environment. We discuss the importance of our results for the future fabrication of atomic-scale devices in silicon.

Keywords: Scanning tunneling microscopy; Nanoelectronics; Silicon; Lithography

1. Introduction

The annual turnover of the electronics/semiconductor industries is over 1 trillion dollars constituting 10% of the gross domestic product of the planet. The driving force for the continued expansion of the microelectronics industry is the ability to pack even more features onto a silicon chip, achieved by continual miniaturisation of the size of the individual components. Over the past three decades, this trend, known as "Moore's Law" has continued with the number of components on a chip doubling roughly every 18 months. Current state-of-the-art optical lithography used in commercial semiconductor manufacturing produces feature sizes down to ~90 nm [1]. However, if device miniaturisation continues at the same rate then by 2017 commercial device sizes will reach the sub nanometer scale. To date, the only tools that have allowed the manipulation of matter at the atomic level are scanning probe microscopes. Since its invention in the 1980s [2], the scanning probe microscope has been adapted as a tool to manipulate atoms on surfaces. This has been particularly successful for the manipulation of absorbates on metal surfaces [3]. However it has not been so easy to manipulate atoms on a semiconductor surface due to the strong covalent bonds involved.

In 1994, Lyding *et al.* proposed a method to achieve atomic resolution lithography in silicon by using a scanning tunneling microscope (STM) to pattern a resist layer on the silicon surface—analogous to that used in conventional optical lithography [4]. In this work the surface of silicon was passivated with atomic hydrogen as the resist in ultra high vacuum. The tip of a STM was used to remove hydrogen atoms from the resist, thereby exposing the reactive underlying silicon surface. The vacuum system was then flooded with gases of different species, which adhered to the silicon surface at the reactive dangling bond sites. This method has since been successfully adopted by numerous groups for the creation of patterned nano-scale features on the silicon surface for the adsorption of oxygen [4], ammonia [5], iron [6], aluminium [7], gallium [8], cobalt [9], silver [10], $TiCl_4$ [11], and large organic molecules, see for example, norbornadiene [12] and styrene [13].

Recently, there has been a growing interest to incorporate STM-based lithography into proposals for atomic-scale semiconductor device fabrication [14–17]. In 1998 Tucker and Shen proposed using PH_3, AsH_3 or B_2H_6 as a precursor dopant source in silicon [15]. Since this time our group has adopted this approach for the realisation of nano and atomic-scale devices in silicon using scanning tunneling lithography combined with low temperature silicon MBE and phosphine (PH_3) as the dopant source. This review will summarise our results for developing a complete strategy for atomic-scale device fabrication in silicon. In particular, we highlight how we have overcome some difficult technological challenges to

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achieve this, including the ability to identify single P dopant atoms in silicon, to place P dopants in silicon with atomic precision, encapsulate them in epitaxial silicon with minimal segregation/diffusion and devise a registration technique that allows the alignment of macroscopic surface electrodes to contact the buried STM-patterned P nanoscale device elements. The fabrication strategy we have developed shows immense promise for increasing our understanding of devices with controlled dopant profiles and for the realisation of more sophisticated atomic-scale devices in silicon such as single electron transistors (SETs) [18], quantum cellular automata [19] and a Si based solid-state quantum computer [20].

2. Overall fabrication strategy

Over the past few years we have developed a detailed fabrication process for atomic-scale devices in silicon with a STM using the strategy outlined in figure 1. Initially registration markers are etched into the silicon substrate that are subsequently used to align the STM-patterned buried dopant layer to surface electrodes. Optimisation of STM-based hydrogen lithography (figure 1b) down to the atomic-scale has enabled us to adsorb single PH_3 molecules at selective sites on the silicon surface [17]. A critical anneal controllably incorporates individual phosphorus dopant atoms from the PH_3 molecules into the silicon surface with atomic precision [21,22] (figure 1c) before thermally removing the hydrogen resist (figure 1d). In parallel, separate studies have shown that a sheet of phosphorus atoms can be encapsulated using MBE (figure 1e) at low temperatures [23,24] to minimise dopant diffusion and segregation. Finally the sample is removed from the ultra-high vacuum STM and the registration markers are used to align surface electrodes to the buried dopant layer (figure 1f). This strategy has allowed us to fabricate nanoscale devices in silicon and characterise their electrical quality outside of the ultra-high vacuum microscope environment. The following sections will describe some of the key fabrication challenges that have been overcome to achieve this.

3. Registration markers for robust STM-patterned devices

Whilst the ability to fabricate nanometer and atomic-scale electronic device structures in silicon by STM has long been promised, the realisation of robust devices has been

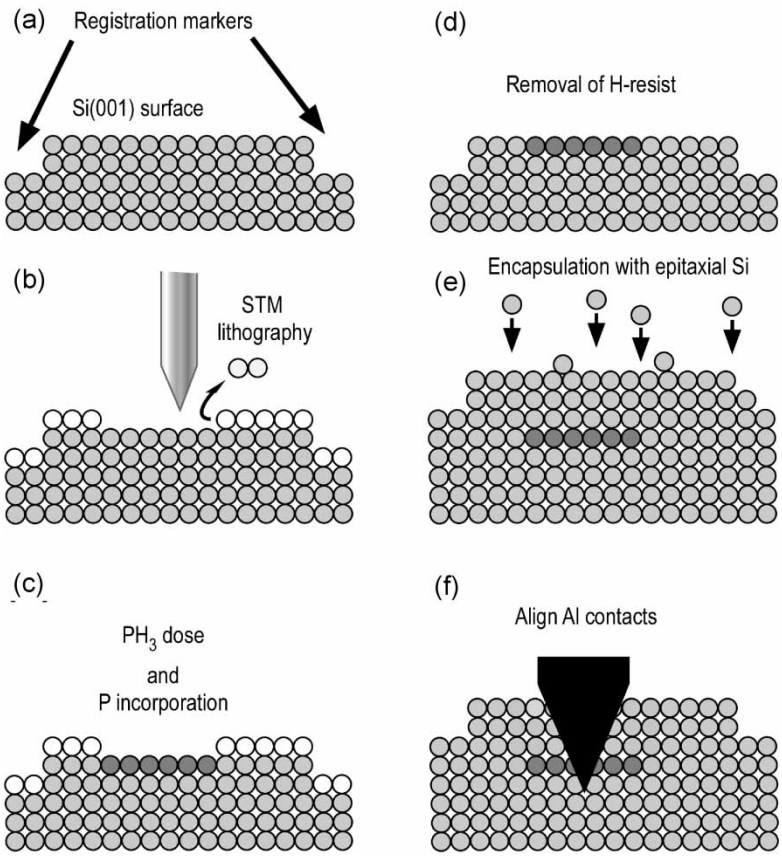

Figure 1. A complete device fabrication strategy for the creation of Si:P atomic and nano-scale devices using scanning probe microscopy. Cross-sectional schematics of essential fabrication steps, including (a) the formation of an atomically flat Si(100) surface with registration markers, (b) using the STM tip for lithography after hydrogen terminating the surface (c) dosing with PH_3 and annealing the patterned surface to incorporate the P atoms into the surface (d) removal of the hydrogen resist before (e) encapsulation with epitaxial silicon grown by MBE and (f) alignment of surface electrodes using the prepatterned registration markers to the buried P layer to make electrical contact.

a difficult goal to attain because of the engineering problem of making electrical contact to the STM-patterned buried dopant layer. The problem is that once the sample is removed from the ultra-high vacuum where STM lithography has taken place the actual location of the structure is lost. This is particularly the case when the nanostructured regions are buried under several layers of epitaxially grown silicon. To this end, we have developed a registration technique where markers, defined by conventional optical lithography, are etched into the substrate before loading into the vacuum for STM patterning [25,26]. To facilitate the ease of using optical lithography on silicon samples we have designed the STM system to take large $1 \times 1\,\mathrm{cm}^2$ samples. After etching, the silicon substrate is thoroughly cleaned to completely remove the optical resist before loading into the STM. Figure 2(a) shows an SEM image of a series of markers that have been patterned and etched to a depth of $\sim 300\,\mathrm{nm}$ into silicon using a tetramethylammonium hydroxide (TMAH) anisotropic wet chemical etch. Different size features are used for alignment of the final device: $1 \times 1\,\mu\mathrm{m}^2$ markers are used to align the STM tip to pattern the dopant layer with respect to the markers, see figure 2(a,b) and markers up to $50 \times 50\,\mu\mathrm{m}^2$ in size are used to align surface ohmic contacts defined by optical lithography to the buried STM-patterned regions, figure 2(c). Once loaded into the vacuum system the sample is heated to $\sim 1050^{\circ}\mathrm{C}$ for 10 s using an electron beam heater to give the Si(100)2×1 surface reconstruction. Most importantly we find that after heating the registration markers survive with very little change and at the same time, we can still achieve atomic resolution imaging of this surface. This confirms that the substrate has not been contaminated during the optical processing steps with the use of resists prior to loading into the vacuum system.

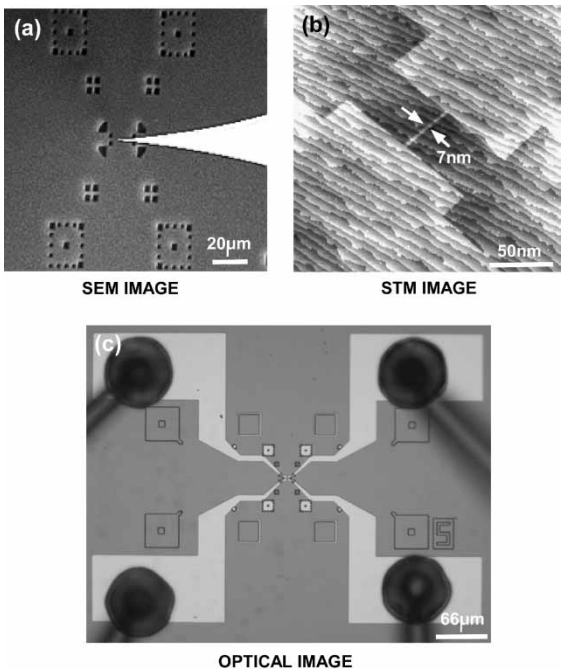

Figure 2. Aligning STM-patterned buried dopant layers to surface electrodes: (a) an SEM image of the registration markers etched into the silicon substrate, (b) a filled state STM image of a hydrogen terminated surface that has been patterned into a quantum wire using the STM tip and registered to the markers and (c) an optical image of the final bonded device where ohmic contacts have been aligned on the surface to the buried STM-patterned quantum wire using the etched markers.

The surface is then hydrogen terminated by exposing it to atomic hydrogen from a cracker source whilst heating the substrate to $\sim 350^{\circ}\mathrm{C}$ at a pressure of $\sim 10^{-7}\,\mathrm{mbar}$. After termination, the tip of the STM is used to selectively desorb hydrogen atoms by applying bias voltages of ~ 6–$7\,\mathrm{V}$ and tunneling currents of ~ 3–$4\,\mathrm{nA}$ to form the device pattern. Figure 2(b) shows a typical STM image of a quantum wire (in this case 7 nm wide) that has been patterned into the hydrogen resist. The bright regions correspond to areas where the hydrogen has been desorbed exposing the underlying silicon dangling bonds. From this image it is also possible to discern the atomic steps on the surface. At the ends of the wire we pattern additional large rectangular regions ~ 3–$5\,\mu\mathrm{m}$ in dimension. These large areas will subsequently be used to contact the buried device. Once the patterned layer is dosed with PH_3, annealed and overgrown with silicon, the device is removed from the vacuum system and aluminium contacts are evaporated above these 3–$5\,\mu\mathrm{m}$ patches using optical lithography. The device is annealed to $\sim 350^{\circ}\mathrm{C}$ for 15 min so that the aluminium diffuses down and make an ohmic contact with the buried STM-patterned phosphorus layer. An optical microscope image of the final device, with gold ball bonded wires is shown in figure 1(c).

The images in figure 2 highlight the range of technologies that have been aligned compatibly, from nanoscale STM imaging to larger, micron scale SEM imaging and finally 100 micron optical imaging. A key feature of this registration process is that it is compatible with atomic-scale device fabrication since the STM can perform both atomic and large micron sized patterning thereby bridging the gap between these two length scales. We can therefore use standard optical lithography to make electrical contact to the large buried contact pads and also use the STM to pattern atomic features between the pads thereby avoiding the issue of directly contacting buried nanoscale features.

In summary, this technique offers an absolute method of registration that allows nano and atomic-scale features to be relocated after each stage of the device fabrication process. We can produce many different devices on the same chip and can contact each device individually thereby providing an independent method of testing the success of each of the various stages of the fabrication process. In addition, we are currently optimising this technique to allow the registration of nano-scale surface electrodes to the active region of buried devices. Ultimately it will also lead to multi-level STM patterning, that combined with MBE growth, will give atomic resolution in all three spatial dimensions to form truly 3D atomic-scale devices.

4. Identification of atomic-scale features in silicon

To adapt this fabrication strategy down to atomic-scale devices in silicon, where individual phosphorus dopant atoms are used, it is necessary to develop both the ability to identify single atom features in STM imaging and a detailed understanding of the surface chemistry. This is particularly the case when we want to be sure of the exact number of dopants in the device—what is the signature of a single phosphorus atom in the silicon surface? In our experiments we have used PH_3 gas as the dopant source. Figure 3(a–d) shows a representative STM image of Si(100)2 × 1 surface after it is dosed with <0.001 L PH_3 showing numerous different surface species and highlighting the complexity of the surface chemistry. The underlying silicon dimer rows can clearly be identified. Additionally, there remain numerous features related to the dissociation of PH_3 on the surface. Whilst it has been well established that PH_3 adsorbs dissociatively on the Si(100) surface at room temperature [27] there have been conflicting reports as to the identification of the numerous intermediate species observed in the STM imaging. To identify these features we have performed an extensive experimental study in combination with a detailed theoretical *ab initio* survey of all the possible dissociation products [28]. From these works we have identified the most prominent phosphorus containing species on the surface as PH_2, PH and P (figure 3(b)–(d), respectively). This is the first step to understand how to identify a single phosphorus atom on the surface using STM. However for the fabrication of atomically precise dopant profiles we would need to be able to identify the signature of a phosphorus atom in, and ideally under the surface to prove that it has remained in position during all the fabrication steps.

In particular, we want to ensure that any device feature we have patterned with the STM is not destroyed during subsequent device fabrication steps such as encapsulation with epitaxial silicon. To minimise phosphorus diffusion/segregation we have performed an annealing step to incorporate the P atoms from the PH_3 molecules into the Si(001) surface while leaving the surrounding hydrogen terminated surface intact. Previous studies have shown that upon annealing PH_3 dosed surfaces to ∼550°C the phosphorus atoms from the dissociated PH_3 molecules substitute for surface silicon atoms to form Si—P heterodimers [24,29]. However, at this temperature hydrogen is also desorbed from the surface indicating that this anneal temperature would be incompatible with the hydrogen resist technology. As a consequence, we have investigated annealing the surface at ∼350°C to incorporate the phosphorus atoms whilst keeping the temperature below the hydrogen desorption temperature [30]. Figure 3(e) shows a filled state STM image of a 0.01 L PH_3 dosed surface that has been annealed to 350°C. The most apparent feature in this image is the bright, short, thin one-dimensional lines above the surface, which correspond to rows of silicon dimers that have been ejected from the surface during phosphorus incorporation. Figure 3(f) shows these chains in more detail where their apparent height (∼0.14 nm) and orientation with respect to the underlying dimer rows confirms this identification. The presence of ejected silicon is a promising sign that phosphorus atoms have incorporated into the surface; however, they remain difficult to observe since they are overshadowed by the bright silicon chains. By contrast-enhancing the image we are able to resolve the characteristic asymmetric signature of a single phosphorus atom in the surface—forming a Si—P heterodimer in figure 3(g). In addition we also observe dark, single dimer vacancy like features on the surface corresponding to hydrogen terminated silicon dimers (H—Si—Si—H) which form as a result of dissociation of phosphine. These studies have demonstrated that we can identify the different phosphorus-related species on the surface and more importantly, have a definitive signature of a single phosphorus atom in the silicon surface.

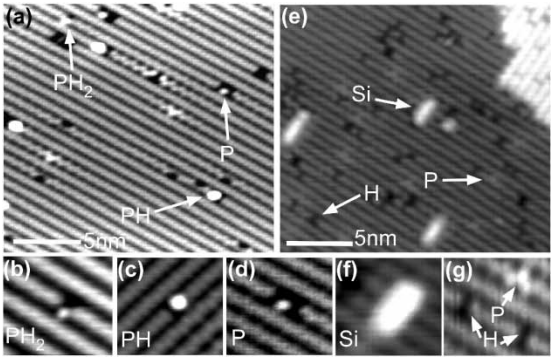

Figure 3. Identification of atomic-scale features on the silicon surface: (a) a filled state STM image of the Si(100) 2 × 1 surface after room temperature dosing with PH_3 showing high resolution filled state images of (b) PH_2 (c) PH and (d) P on the surface. (e) This shows the surface after an anneal to 350°C highlighting (f) the ejected silicon dimer chains and (g) a Si—P heterodimer and monohydrides on the surface.

5. Atomic precision placement of individual P atoms in silicon

The next important question is whether the incorporation of the phosphorus atom with this anneal step at 350°C is compatible with the hydrogen resist technology. Do we have the ability to control the incorporation of a single phosphorus atom in the surface with atomic precision using the hydrogen resist strategy? Figure 4(a) shows a hydrogen terminated surface with a controlled desorption site of 1 nm diameter fabricated by pulsing the STM tip. Figure 4(b) shows the same area of the surface after dosing with ∼0.3 L PH_3 and annealing to ∼350°C. In this image we can see two things. Firstly, we can see a very clear signature of the asymmetric P—Si—H heterodimer within the lithographic area, and secondly the hydrogen atoms from the dissociated PH_3 molecule have reterminated the lithographic area [21,22]. This result is important since it confirms the ability to spatially control the incorporation

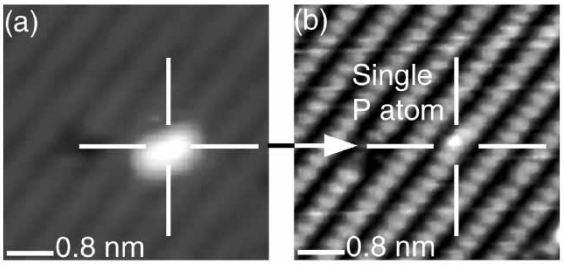

Figure 4. STM images of atomically controlled single P atom incorporation into Si(100). (a) hydrogen terminated Si(100) with a ~1 nm diameter hydrogen desorption point. (b) the same area after PH_3 dosing and annealing to 350°C showing a single P atom incorporated at the location defined by the hydrogen desorption point.

of single phosphorus atoms in silicon and opens the door to the possibility of creating electronic devices in silicon with atomically controlled dopant profiles.

6. Minimisation of phosphorus segregation

Once an atomically precise array of dopants is fabricated, it is important to encapsulate the array to protect them from defects and surface states which would otherwise disturb their local electronic environment. This poses a problem—it is important to ensure that the dopants are encapsulated in high quality epitaxial silicon to avoid the presence of defects. Defects such as vacancy interstitials are known to enhance dopant diffusion through the silicon crystal [31]. However, high quality silicon epitaxy is generally achieved at high growth temperatures, typically >650°C (in the step flow regime). At these temperatures, the silicon adatom mobility is high and any voids and vacancies in the crystal that occur during growth are filled in, leading to the formation of complete terraces [32]. The problem is that at these high growth temperatures the phosphorus dopants are also likely to segregate [33] and diffuse through the silicon [34] thus destroying the carefully created STM-patterned array.

It is possible to grow epitaxial silicon at room temperature up to a certain critical thickness, h_{epi} after which it becomes amorphous [35,36]. This critical thickness is dependent on both growth temperature and growth rate [37]. At room temperature and a growth rate of 0.7 Å/s they found the value of h_{epi} ~10 Å. At higher growth temperatures the critical thickness increased for example, at 250°C the critical thickness h_{epi} was found to be ~30 nm for the same growth rate. Additionally, if we decrease the growth rate of the silicon the value of h_{epi} becomes larger . It is therefore necessary to optimise the growth conditions for the silicon encapsulation layer to produce a high quality crystalline layer but also to minimise both the phosphorus segregation and diffusion.

To characterise the degree of vertical segregation we fabricated a series of three phosphorus in silicon δ-doped samples, A, B and C at different overgrowth temperatures (RT, 250°C and 400°C) for a fixed silicon growth rate of ~0.05 Å/s. Figure 5 describes the sample preparation procedure along with filled state STM images of each of the fabrication steps. Figure 5(a) shows an STM image of the clean silicon surface. Figure 5(b) shows the same surface after phosphine saturation dosing at room temperature, where it is possible to clearly see the local regions of p(2 × 2) ordering of the adsorbed phosphine. Figure 5(c) shows an STM image of the surface after an anneal at 550°C for 5 min which both incorporates the phosphorus atoms into the surface as described previously and serves to desorb the hydrogen [38]. The resulting density of phosphorus atoms on this surface is ~0.25 monolayers [39] corresponding to a surface concentration of $1.7 \times 10^{14}\,cm^{-2}$. The sheet of phosphorus atoms is now overgrown with ~25 nm of epitaxial intrinsic silicon deposited at a rate of 0.05 Å/s and substrate temperatures of either room temperature (shown in figure 5(d)), 250°C or 400°C. Note that for the room temperature results there was no intentional heating of the sample, however the surface was radiatively heated to several 10°C from the silicon sublimation source. From figure 5(d) we see that the silicon has formed random 3D islands on the surface but that it is still epitaxial as evidenced by the ability to resolve dimer rows.

In order to determine how far the phosphorus atoms have segregated during the encapsulation stage we performed secondary ion mass spectrometry (SIMS) measurements of these samples and the results are summarised in table 1. Detailed analysis of SIMS measurements determined the phosphorus segregation lengths to be ~1.5 nm for the room temperature grown sample and ~2.3 nm for the 250°C sample [40]. For the 400°C encapsulated sample there was

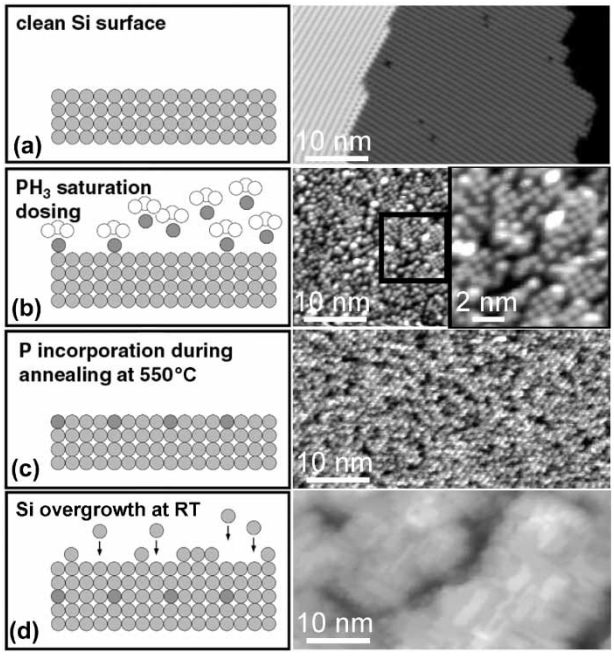

Figure 5. Schematics and STM images describing the sample preparation process for the fabrication of a phosphorus in silicon δ-doped layer used for SIMS analysis to determine segregation lengths and magnetoresistance measurements to determine the degree of electrical activation.

Table 1. The effect of silicon encapsulation temperature on the segregation length, mean free path, phase coherence length, carrier density and mobility of P in Si δ-doped layers.

Sample	*Growth Temp °(C)*	*Growth Rate (Ås^{-1})*	l_{seg}*(nm)*	l_{mfp}*(nm)*	l_{φ}*(nm)*	*ns ($10^{14}cm^{-2}$)*	μ *($cm^2V^{-1}s^{-1}$)*
A	RT	0.05	∼1.5	∼3	52	1.67	∼23
B	250	0.05	∼2.3	∼9	72	1.64	∼61
C	400	0.05	∼100[a]	∼5	21	0.22	∼86

[a]Extrapolation of literature data

significant segregation of the phosphorus dopants towards the surface in agreement with previous studies [33] where the segregation length was estimated to be ∼ 100 nm. At the first glance these results are promising since they seem to suggest that with room temperature encapsulation it should be possible to keep the phosphorus atoms within ∼ 10 monolayers of their original location.

However, we have recently shown that these values can be misleading since it is not possible to detect segregation lengths below the nanometer scale with the resolution limit of SIMS [40]. Instead we have gained a better quantitative estimate of the phosphorus segregation using the STM directly. Figure 3(g) shows the signature of a phosphorus atom in the surface. As a consequence we can encapsulate a Si:P δ-doped layer in silicon grown at different temperatures and observe the increase in number of Si—P heterodimers at the surface when we anneal the surface to different temperatures. Initially we encapsulated a saturation dosed Si:P δ-doped layer at room temperature and then heated the surface to 350°C. We measured the number of phosphorus atoms at the surface and compared this to the number seen after an additional anneal to 400°C. There was only a 1.1% increase in the phosphorus density confirming that the energy barrier of 3.66 eV [34] suppresses phosphorus diffusion at this low temperature. If diffusion at these low temperatures is negligible the presence of phosphorus on the silicon surface after low temperature growth is therefore almost entirely due to surface segregation. From knowing the number of phosphorus atoms on the surface after annealing, it is therefore possible to calculate the segregation length Δ, from knowing the incorporation probability, p_{inc} and the value of $a_o/4 = 0.1358$ nm, the distance between two subsequent Si(100) monolayers [33]. At room temperature Δ was found to be 0.29 nm rising to 0.58 nm at 250°C. These results highlight the effectiveness of room temperature encapsulation to minimise dopant segregation in silicon to within a few monolayers. In addition we have demonstrated how it is possible to quantify the degree of segregation directly using STM. This is a valuable tool if we wish to know the exact number of dopants and their location in the subsequent formation of electrical devices.

7. Electrical quality of silicon encapsulation and phosphorus dopant activation

Encapsulation of the patterned phosphorus dopants in epitaxial silicon also serves to activate the dopants. This is of crucial importance to the operation of devices since the presence of defects is known to severely affect the electrical characteristics of devices [41]. If the phosphorus dopants sit in interstitial or defect sites after the encapsulation process then it is likely that their extra electron will be trapped and not available for conduction. To determine whether the phosphorus atoms sit on substitutional sites after encapsulation, thereby giving up their free electron for conduction we also performed magnetoresistance measurements of samples A, B and C. The results of these studies are summarised in table 1. We can determine the degree of electrical activation by comparing the number of free carriers determined from Hall measurements, n_{s} with the concentration of phosphorus atoms initially deposited on the silicon surface and measured by the STM, $\sim 1.7 \times 10^{14}\,\mathrm{cm}^{-2}$. The carrier densities for samples A and B for room temperature and 250°C encapsulation were found to be constant at $1.7 \times 10^{14}\,\mathrm{cm}^{-2}$ and equivalent to the concentration of phosphorus atoms deposited on the silicon surface. However at 400°C, where the phosphorus atoms were observed to strongly segregate to the surface, the carrier density was observed to decrease to $0.22 \times 10^{14}\,\mathrm{cm}^{-2}$ [42].

As devices down scale in size to the single atom level and below it is important to ensure a complete understanding of key device parameters such as the mean free path and phase coherence length. The mean free path of the electrons, l_{mfp} is the distance between momentum changing collisions and can be determined directly from the mobility, μ of the material. If the mean free path becomes comparable or larger than the sample size then transport becomes ballistic and highly sensitive to boundary conditions (surfaces, contacts and interfaces). The phase coherence length, l_{φ} is another key parameter and represents the average distance an electron will diffuse before undergoing a phase randomising collision. The phase coherence length can be determined from the magnetoresistance of the sample in a magnetic field. If the phase coherence length becomes larger than the sample size then the phase of the particle becomes important and phase interference effects will start to appear in the characteristic conductance of the material.

From the zero field resistivity we were able to extract the mobility for each of the samples and these are shown in table 1. The mobility essentially gives an indication of the degree of disorder in the conduction plane and was found to increase with increasing encapsulation temperature. This is not surprising since the samples grown at higher encapsulation temperatures have a higher crystalline

quality and a reduced density of defects to scatter the electrons. In all cases the mean free path of the electrons is quite small (≤ 10 nm) due to the high density of phosphorus atoms in the 2D plane. To create ballistic devices therefore we would need to make samples much smaller than this length scale.

A detailed analysis of the magnetoresistance data [42] allowed us to extract the phase coherence length, l_φ at 4 K for these samples which is again summarised in table 1. Here we can see that value of l_φ is peaked at ~ 70 nm for the sample encapsulated at 250°C. The peak in l_φ arises because $l_\varphi \propto (\pi m_s \tau_\varphi)^{1/2}$, where τ and τ_φ are the corresponding momentum and phase relaxation times, such that if we increase the encapsulation temperature, τ increases and l_φ also increases. However at the highest encapsulation temperature, the carrier density, n_s decreased dramatically offsetting the rise in τ, leading to the reduction in l_φ. Since the phase coherence length is strongly dependent on temperature [43], increasing as the temperature is reduced, our results highlight that novel devices that exploit the quantum coherence of electrons should be possible even with a device length of ~ 100 nm. More detailed studies are underway in our group to further increase the mean free path and phase coherence length in these Si:P δ-doped layers.

8. Minimisation of phosphorus diffusion

Whilst it has been possible to determine the degree of phosphorus segregation at room temperature directly using the STM it is much more difficult to determine the degree of lateral phosphorus diffusion. To achieve this, we really need to observe the phosphorus atoms underneath the surface after encapsulation to show that they haven't moved. The imaging of buried dopants has been previously achieved for B [44] and A's [45] in silicon. Here the dopant atoms present in subsurface layers can locally induce band bending which changes the tunnel current between the sample and the STM tip. The consequence of this is that buried dopants can appear as enhancements or depressions superimposed on the periodic surface lattice depending on the bias polarity and sign of the dopant charge. Random buried phosphorus dopants have also been observed in clean, bulk doped silicon that has been flash annealed [46]. The appearance of the buried dopants are strongly affected by the termination of the silicon surface. A bare silicon surface contains surface states causing Fermi level pinning thereby making it difficult to see the effect of the buried dopants. This effect of the surface states can however be removed from the band gap by terminating the surface with hydrogen [47].

To investigate the possibility of measuring buried phosphorus dopants under the silicon surface, we prepared several PH_3 dosed surfaces of different phosphorus density. We annealed the samples at 600°C for 1 min to incorporate the phosphorus atoms into the silicon surface and desorb the remaining hydrogen. The surface was then encapsulated with 10 monolayers of silicon grown at room temperature at a growth rate of 0.5 Å/s before being annealed at 450°C for 5 s to flatten the surface. Finally the surface was hydrogen terminated at a sample temperature of 325°C.

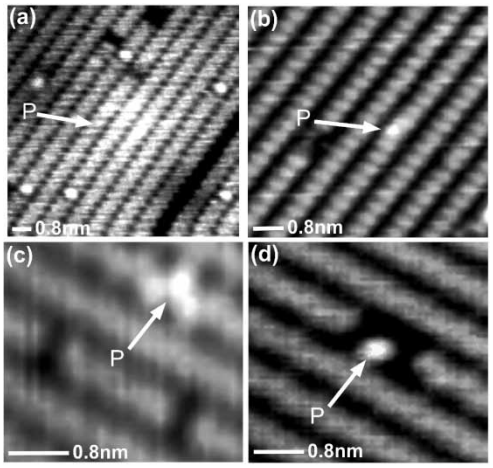

Figure 6. Signatures of a single phosphorus atom in silicon observed (a) under 10 monolayers of epitaxial silicon, (b) on a hydrogen terminated surface, as a hydrogen terminated Si—P heterodimer (c) as a heterodimer in the silicon surface and (d) as a single P atom adsorbed to the surface after PH_3 dissociation.

Figure 6(a) shows an empty state image (+1.8 V) of a surface that has been exposed to PH_3 for a few seconds at a pressure of 5×10^{-10} mbar before encapsulation and hydrogen termination. Across the surface we can identify a known density of single buried phosphorus atoms under the hydrogen terminated surface that is observed to scale with the density of phosphorus atoms deposited. These buried atoms are identified as enhancements superimposed on the dimer structure, which extend over two or more dimer rows in diameter. Interestingly, the phosphorus dopants appeared very bright in empty state imaging but only showed a very faint protrusion in filled state images [48]. The results shown in figure 6 highlight the identification of a single phosphorus atom in silicon at all stages of the device fabrication process from (a) under the surface, (b) in a hydrogen terminated surface, (c) in a clean silicon surface and (d) on top of the silicon surface. This final step of characterising the appearance of the phosphorus atom beneath the surface is crucial to determine if the dopants diffuse out of the areas where ordered arrays have been fabricated using STM lithography. It should be noted that whilst it is only possible to image the dopants a few monolayers beneath the surface, the phosphorus atom is unlikely to change its position significantly during further low temperature encapsulation.

Preliminary studies have commenced to determine if an array of phosphorus atoms patterned by STM lithography can be imaged after silicon encapsulation at room temperature. Figure 7(a) shows a filled state STM image of a hydrogen terminated surface where the STM tip has

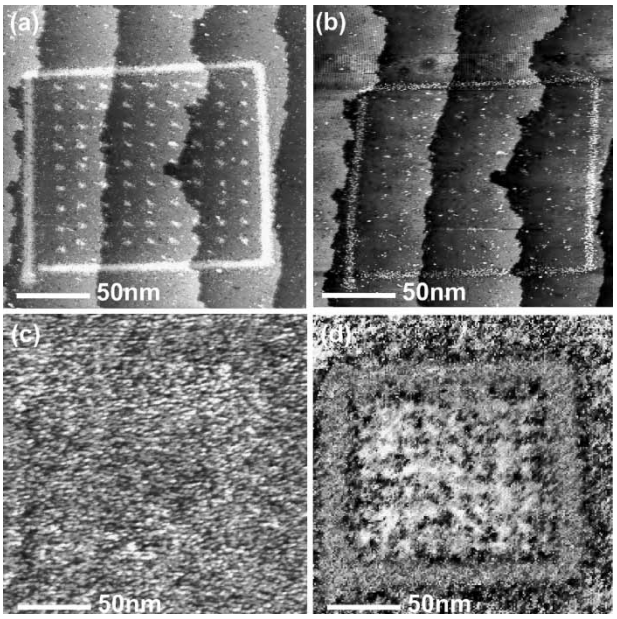

Figure 7. Preliminary studies into the lateral diffusion of a phosphorus array encapsulated in silicon at room temperature. (a) A filled state STM image of a H-terminated Si(100) surface where the STM has been used to remove hydrogen atoms to form a 9×9 array of desorption sites $\sim$6 nm in diameter surrounded by a box of $\sim$6 nm line width. (b) The same surface after PH_3 dosing and annealing to 380°C for 5 min. (c) After encapsulation with 1–2 monolayers of silicon encapsulation at room temperature and a further anneal at $\sim$380°C for 5 min and (d) an STS image of the same surface.

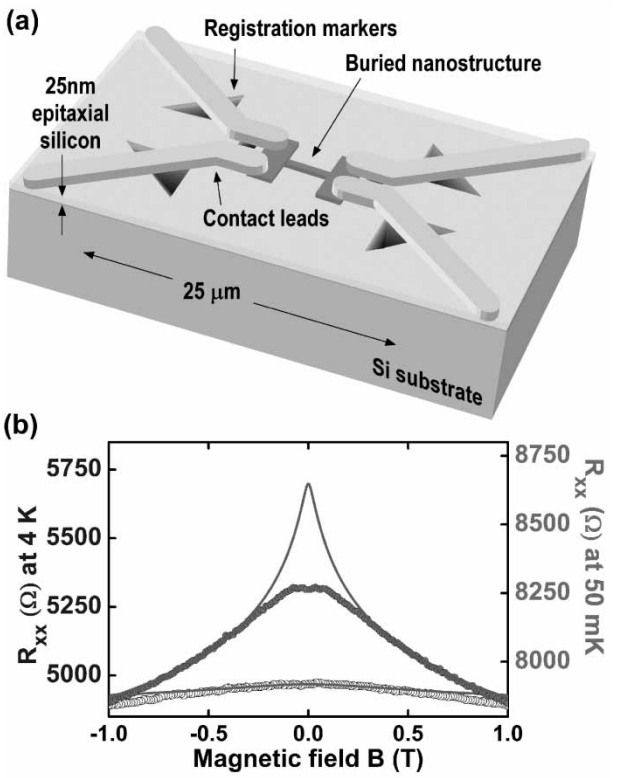

Figure 8. (a) A schematic of a $90 \times 900\,nm^2$ quantum wire patterned by STM showing triangular registration markers etched into the silicon substrate. Aluminum ohmic contacts (shown in yellow) were fabricated by optical lithography after removing the sample from the STM–MBE system. (b) Electrical measurements showing the magnetoresistance of the $90 \times 900\,nm^2$ wire at 4 K (blue line) and 50 mK (red line). The turquoise-green lines show fits to 2D weak localisation theory.

been used to depassivate a square line of thickness $\sim$6 nm around a 9×9 array of $\sim$6 nm patches, allowing the adsorption of $\sim$10–20 phosphine molecules in each patch. Figure 7(b) shows the same area of the surface after a saturation dose of phosphine followed by an anneal at $\sim$380°C for 5 min. Here we can clearly see signs of phosphine dissociation as evidenced by the retermination of the patches. After 1–2 monolayers of silicon encapsulation at room temperature and a further anneal at $\sim$380°C for 5 min, the resulting filled state STM image of the surface in shown in figure 7(c). There appear to be no signs of the array. However silicon growth at room temperature is known to be extremely rough due to the random formation of 3D islands and it is not surprising that even after an anneal, this roughness would mask the appearance of the buried dopants using this mode of constant current imaging of the STM. However, it is also possible to position the tip at some fixed lateral position and perform an I-V measurement giving information on the spectrum of states over the applied voltage range. This form of imaging is called current imaging tunneling spectroscopy (CITS) and the resulting image at a bias of -1.8 V is shown in figure 7(d). From this image we can clearly see that the dopants are still visible. However it is difficult to say at this stage whether the dopants have laterally diffused a few nanometers during the room temperature silicon encapsulation step and subsequent anneal, or whether the signal has smeared out by to either the large number of phosphorus atoms present or the fact that the STM tip is further away from the donors. Current studies are underway to quantify the degree of lateral diffusion under different encapsulation conditions [49].

9. Electrical characterisation of a STM-patterned nanoscale quantum wire

Over the past few years our group has overcome several challenges to the realisation of nano and atomic-scale devices in silicon using the strategy outlined in figure 1. Most recently this has resulted in the fabrication of a $90 \times 900\,nm^2$ quantum wire device patterned by STM lithography, see figure 8(a). Here we have utilised etched registration markers, STM lithography to create the nanostructure, a critical anneal to incorporate the donors and low temperature silicon encapsulation to complete the device before aligning surface ohmic contacts to the buried layer [25]. Importantly we are able to image the device at each stage of the fabrication process and identify the location of the dopants.

Four terminal magnetoresistance measurements of the device were performed at 0.05–4 K to confirm the suitability of the fabrication strategy for the creation of nano-scale devices. In figure 8(b) we show the 4 K magnetoresistance of the quantum wire which shows a peak centered around $B = 0$ (blue trace) that becomes more pronounced as the

sample is cooled to 50 mK (red trace). This temperature-dependent magnetoresistance is a characteristic signature of weak localisation arising from coherent backscattering of forward and time-reversed electron waves around a loop as electrons diffuse through the sample. We can extract the phase coherence length of the electrons by fitting the magnetoresistance to the Hikami [50] expression for weak localisation in the diffusive regime (see turquoise-green lines). At 4 K the phase coherence length extracted $l_\varphi = 32$ nm is smaller than the width of the wire.

As the temperature is reduced to 50 mK the fit of the Hikami expression (turquoise-green trace) to the experimental data (red trace) deviates at magnetic fields below ~ 0.3 T. If we extract the value of the phase coherence length from this fit we can see that it has increased to $l_\varphi = 135$ nm. This value of l_φ is now larger than the wire width such that the lateral dimension of the wire limits the maximum size of electron loops that can contribute to weak localisation. Thus although the negative magnetoresistance becomes stronger in the wire as T is reduced as expected, it does not produce such a pronounced peak around $B = 0$. This suppression of the 2D weak localisation around $B = 0$ is a direct signature of the crossover from two-dimensional to one-dimensional electron transport as the temperature is reduced.

We can use this suppression of the 2D weak localisation to independently measure the width of the quantum wire from the electrical measurements, and compare it with the STM lithography and imaging. As the magnetic field increases the size of the constructively interfering loops becomes smaller, so that it is B, and not the wire width, w that determines the magnitude of the weak localisation effect at 50 mK. Thus the wire approaches two-dimensional behaviour when $2l_B \sim w$, where l_B is the magnetic length. From figure 8 we see that the measured 50 mK data merges with the green line of the 2D theory at $|B| \sim 0.3$ T, giving a wire width of ~ 90 nm, in excellent agreement with the STM-defined geometry. The results obtained for this device demonstrate the power of using scanning probe microscopy to fabricate electronic devices, not only does it allow the patterning of conducting regions with atomic-resolution but it is also possible to image the active region of the device during the fabrication stages thereby confirming the size (and ultimately number of dopants) in each device. The demonstration of this fabrication technology, and the successful measurement of a STM fabricated device, will in future allow us to design devices with atomic accuracy and see the effect the individual dopant placement has on the device characteristics.

10. Conclusions and future device directions

We have demonstrated a novel strategy for fabricating nano-scale devices in silicon using a STM. This strategy, whilst demonstrated for nano-scale devices, also shows immense promise for the realisation of atomic-scale devices in which controlled dopant profiles are required. Using the technology we have developed it should be feasible to control the exact position and number of phosphorus dopants using STM and investigate the effect this has on the device characteristics. Figure 9 gives an insight into the range of devices that can be fabricated from (a) single dopant atom wires to (b) nanometer quantum wires to (c) ordered arrays of dopants.

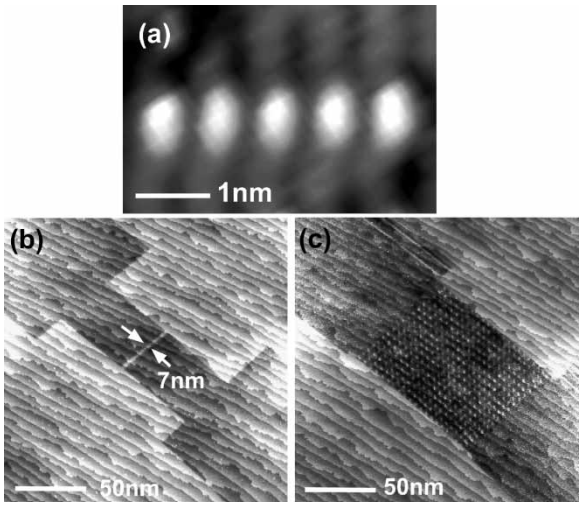

Figure 9. STM images of novel device structures on a hydrogen terminated silicon surface in which we have (a) selectively removed five individual hydrogen atoms with atomic precision for the creation of precise linear arrays of dopants, (b) desorbed a 7 nm wide quantum wire and (c) created a 2D array of dopants with a 5 nm dot size and 10 nm pitch.

The route to future device miniaturisation will require means other than simple scaling or device improvements. One such route is to explore the third dimension more effectively. Whilst integrated circuit technology has traditionally been planar, it is possible using our approach to build several layers on top of one another. Ultimately the goal will be to realise sophisticated atomic-scale devices in silicon such as SETs, quantum cellular automata and a Si based solid-state quantum computer.

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